Improving Quality and Yield Through Optimal Big Data Analytics

International Test Conference

October 2015
# Marvell at Glance

- **Founded in 1995 by three UC Berkeley engineers**
- **IPO on June 27, 2000**
- **Operating headquarters in Santa Clara, CA, USA**
- **Annual revenue of $3.7B (end of FY15)**
- **7,000+ employees (end of FY15)**
- **Approximately 1B chips shipment per year**
- **Top 5 global fabless semiconductor company**
- **5,000+ patents filed and 2,500+ patents pending**

## Major R&D Centers
- United States
- China
- Israel

## Global Presence
- India
- Singapore
- Vietnam
- Indonesia
- Taiwan
- Hong Kong
- Japan
- Korea
- Germany
- Spain
- Switzerland
- France
- Sweden
- Denmark
- Italy
- U.K.
Delivering Diverse Product Solutions

- Storage Controllers
- IP/Ethernet Networking
- Embedded Computing
- Broadband Access
- Home Networking
- Wireless Connectivity
- Multimedia Entertainment
- Automotive
- Internet of Things (IoT)
- Smart LED Lighting
- 2D/3D Printing
- Power Management

Advanced Software Technology

Kinoma
Delivering the Industry’s Leading Solutions

#1 in market share for HDD/SSD/Hybrid storage controllers

#1 in market share (40%) for 2D printer digital imaging SoCs

1st ARM-based micro-server storage system

#2 IP/Ethernet networking silicon vendor

#1 Ethernet access silicon vendor

2nd generation Android TV HD multimedia SoC provider
Marvell Supply Chain
Operations Background
(Where We Were in 2012)

• Marvell manufacturing 1B+ units per year

• Existing “systems” in place
  – Labor-intensive, but they were working

• The Ops team identified several areas for improvement
  – Faster access to manufacturing data
  – Ability to drill down across all products and test domains
  – Automated data analytics, plots and alerts for all devices
  – Better, data-driven internal communication across company sites
  – Better, data-driven external communication to subcons
Implemented Optimal+ In 2013

Marvell Subcons

Marvell Headquarters

- CLIENT APPLICATIONS
  - Analytics
  - Queries
  - Rules
  - Simulations

APPLICATION SERVERS

OPTIMAL+ DATABASE

Alerts & Linked Reports

Guidance & Requests

MES

DATA

Data

Data

Real-Time

OPERATIONS CLIENT

PROXY SERVER

Wafer Maps

Bin Switch

Wafer Test

WAFER SORT TESTER

FINALE TEST TESTER

Marvell Subcons

Marvell Headquarters
Optimal+ Provided Early Successes

- Yield Improvement
Optimal+ Provided Early Successes

- Improvements in Throughput and Capacity
Unexpected Findings and Benefits

• Very little cross-company learning for subcons already supporting Optimal+
  – No sharing of information about best-practices

• Optimal+ found some basic issues that should not have been there in the production line
  – Despite tools in place at subcons that should have detected the problems.

• Big Data benefits that were unforeseen during pilot
  – Duplicate ECIDs (electronic chip IDs)
  – Ugly wafers
  – Improvements in “institutional knowledge”
Duplicate ECIDs
Serious Product Issue at EMS

• Trigger event: In early 2015, one of our customer’s EMS reported “off the charts” DPPM for an assembly lot
  – Error code was related to data programmed by Marvell at the unit level
  – EMS readied the units to be returned to Marvell’s FA team

• At the same time, Marvell’s Product Engineering team reviewed the lot and manufacturing history using O+
  – All general indicators were normal (yield etc.)
  – Product engineer did a simple “drill down” into the manufacturing data which quickly uncovered an ECID anomaly
  – 151 repeated instances of same ECID at Final Test, but not in Wafer Sort

<table>
<thead>
<tr>
<th>ECID Analysis</th>
<th>Final Test Max Instances of ECID</th>
<th>Wafer Sort Max Instances of ECID</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOT_abc_Z17</td>
<td>151</td>
<td>1</td>
</tr>
<tr>
<td>All Others</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Rapid Identification of the Problem

• ECID Sequence Plot clearly showed an anomaly
  – No other repeated ECIDs observed in this Lot other than the one below

• Likely cause was a “piggybacking” event

ECID Plot in Test Sequence
Same ECID repeated Sequentially

Final Test IC Touch Down Sequence
Root Cause Analysis

- Ops looked at the “Index Time” between each unit
  - Test iterations between the 2 long pauses = the # of ECID’s repeated

- Wafer Level data showed no repeated ECID
  - This data result is not possible without a Piggyback event
Key Takeaways

• Quantum improvement in debug of difficult FA
  – Abnormality observed within 15 minutes
  – Root Cause determined in 1 hour
  – Engineering work completed in <1 day, 6,000 miles from occurrence
    • Risk assessment on the 4.5M units already shipped
  – Corrective / Preventative Action in place 1 week after diagnosis

• Significant FA work and time saved
  – Mobilizing QA team
  – Cycle time of doing general FA (shipping, testing, etc.)

• Automated signature detection rule was implemented to immediately recognize this problem in the future

• All addressed using Optimal+
“Ugly Wafer” Detection using Escape Prevention
Escape Prevention Solution

• In early 2015, Marvell was in the process of implementing the Optimal+ Escape Prevention solution to improve overall product quality by reducing test escapes

• The Escape Prevention solution included 3 families of Outlier Detection capabilities:
  – Parametric, Geographical & Cross-Operational

• The solution was already embedded into ALL major foundries & OSAT operations used by Marvell

• The combination of Escape Prevention and comprehensive production data enabled Marvell to find expected and unexpected things
Expected Results: GDBN & Clusters
Other Expected Results: Clusters
Observations using Escape Prevention

• While tuning EP rules, the Marvell Ops team detected “unusual defect patterns” on the wafers
  – Easy to see visually, difficult to detect algorithmically

• Marvell worked with Optimal+ to enhance our existing algorithms to automatically identify the wafer defects that were discovered
  – Fully automated process that could run on every manufactured wafer

• This finding prompted Marvell to establish a new metric for Subcon communication: The “Ugly Wafer” metric
Wafers with “Unusual Defect Patterns”

Easy to identify visually, but hard to identify automatically when looking at data with an algorithm.
Ugly Wafer Metric

- After realizing the number of “scratched” wafers being delivered, Optimal+ worked with Marvell to enhance the existing algorithms to automatically identify these “ugly wafers”

- Results are tabulated into a quantifiable metric that is used in discussions with fabs during QBRs
Key Takeaways

- Automated detection of “ugly wafers.”
  - Run on 100% of sorted wafers
  - Real time detection
  - Allows quick disposition and feedback to foundry

- Throughput improvement of detection of “ugly wafers”
  - Marvell makes 1B units a year, 1000 wafer lots a month, lots of work if done by hand
  - Human inspection is inefficient and error prone
  - Fatigue is a major factor in missing a pattern

- Completely facilitated by O+ rule implementation.
Better Communication
Improved Communications: Consistent Data Shared Internally and Externally

**Same data shared** between engineering, operations, planners, finance and management
Future Directions of Marvell
Driving Continuous Innovation

**FLC™ (Final-Level Cache)**
- Significantly reduced memory size
- Optimized energy efficiency
- Reduced form factor

**MoChi™ (MOdular CHIp)**
- Quick time-to-market
- Flexible configuration for targeted applications
- Reduced R&D cost via reusable functions
MoChi™ (MOdular CHIp)

MoChi™: A MOdular Chip concept that can be configured like a Lego® set, providing flexibility in design and functionality compared to conventional Single-Die SoC approaches.

Diagram:
- **Single-Die SoC:**
  - GPU
  - CPU
  - WiFi
  - USB
  - MODEM
  - G.hn

- **Virtual SoC:**
  - Lego®-like concept with components including:
    - South Bridge
    - Application Processor
    - DRAM
    - Daisy Chain Connection
    - DRAM Access
    - Point-to-Point Connection

This diagram illustrates the transition from a conventional Single-Die SoC to a Virtual SoC that emulates the modular and versatile nature of Lego® sets, offering greater configurability and adaptability in semiconductor design.
Final-Level Cache (FLC™)

Conventional DRAM

Now

CPU

L1 Cache
L2 Cache
L3 Cache

DRAM

Future

CPU

L1 Cache
L2 Cache
L3 Cache

High Speed

Stage 1

Stage 2

Flashing

Main Memory

FLC

Smaller, Faster, Lower-Power DRAM

Main Memory

Mouse over the diagram to view more details.
Questions?
Thank You!